ABSTRACT

Method and apparatus for implementing a variable length pipeline in a packet-driven memory control system, including a command front end and one or more parallel command sequencers. The command front end decodes an external command packet into an internal command and issues it to a selected one of the command sequencers. The command has associated therewith a desired latency value. A first group of one or more memory control steps for the given command is performed by the command front end if the desired latency value is less than a threshold latency value, or by the selected command sequencer if the desired latency value is greater than or equal to the threshold latency value. The remainder of the memory control steps required for the command are performed by the selected command sequencer. If the first control steps are to be performed by the selected command sequencer, then depending on the desired latency value, the command sequencer further may insert one or more wait states before doing so.